blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock signal, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

4. (ONCE AMENDED) A computer including a main memory and a cache memory, the cache memory being connected to the main memory and divided into a plurality of cache blocks, comprising:

a block state setting unit which supplies a lock signal generated on the basis of a lock instruction to the cache memory to set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited, ; and

a reading/writing unit which performs either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock signal supplied by the block state setting unit, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

13. (ONCE AMENDED) A method of controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory, which is executed by a computer that accesses the main memory through the cache memory, comprising :

determining whether the cache memory is acting as the random access memory; and

assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory,

wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and

wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system

instead of the cache memory.

15. (ONCE AMENDED) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory;

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; and

a selection unit which selects one of a first assignment state and a second assignment state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory.

17. (ONCE AMENDED) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory;

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory;

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received.

18. (NEW) The method according to claim 1, further comprising the operation of